A Large-Signal FET Model Including Thermal and Trap Effects with Pulsed I-V Measurements

Kyoungmin Koh, Hyun-Min Park, and Songcheol Hong
Dept. EECS, Korea Advanced Institute of Science and Technology (KAIST)
373-1, Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea

Abstract — **A large signal FET model is presented. This includes a quiescent bias dependency to predict non-linear dynamic behavior of an FET where thermal and trap effects are present. The intrinsic device of the model is represented by a parallel connection of non-linear currents and charges. The model parameters are extracted from bias dependent pulsed I-V's and small-signal S-parameters. Measurements and simulations of pulsed I-V's and S-parameters have been compared for the verification of the model at various quiescent bias voltages. Also load-pull measurement results including the output power and PAE have been compared to the simulation results for the validation of the non-linear behaviors of the model.**

I. INTRODUCTION

Field effect transistors (FET's) such as MESFET and HEMT have been widely used as power devices in wireless communication area due to their large output power and efficiency. Accurate large signal FET models are absolutely necessary for an optimum design with a short design-to-production cycle.

Despite the superior RF performances, the thermal and trap effects existed in FET devices make the design of power amplifiers cumbersome. These effects severely change the channel current which is the primary source of non-linear characteristics. Therefore it is strongly recommended that these two effects should be predictable by the large signal model for a reliable circuit design.

Pulsed I-V measurements allow the characterizations of device under isothermal and isotrap conditions. Therefore, they have been widely used in the model described in [1-4]. Jastrzebski suggested a new channel current model which consists of reference current function, thermal effect function and trap effect function [1]. Each function was extracted from bias dependent pulsed I-V's. However, it was suggested that the trap effect could be expressed as a function of only quiescent bias voltages. But the trap effect is dependent on both quiescent bias and instantaneous voltages, since it can be affected by the amount of channel current. Fernandez et al. suggested a large signal MESFET model extracted from bias-dependent pulsed I-V measurement [2]. Materka equation was used as a channel current model and each model parameter was expressed as a second order polynomial function of quiescent bias voltages. But they used pulsed I-V's at only 6 bias voltages, which is not adequate enough to express all pulsed I-V's covering a wide range of bias voltages. Ouarch suggested electro-thermal FET model with trap effect [3]. The trapped charges were supposed to act as a pseudo-backgate terminal voltage. But pulsed I-V's at only one power dissipation condition were used for trap effect model. Therefore, it cannot be assured that the model is accurate at other power dissipation condition. A spline FET Model was suggested by the authors [4]. The channel current equation of the model could express all pulsed I-V's covering wide quiescent bias voltage range. However, the model may produce unreliable prediction outside of measurement range unless a proper extrapolation method is used. Also the model needs many model parameters proportional to the size of rook-up table.

In this work, channel current model which can express the thermal and trap effects over a wide range of quiescent bias voltages is presented. A new model parameter extraction method is also introduced to model these effects independently. By using an empirical equation to express the reference channel current, the device can be characterized beyond the measured regions with a small number of model parameters.

II. PARAMETER EXTRACTION PROCEDURE

The device used in this study is GaAs PHEMT with 10 fingers of 0.25 μm gate width and 80 μm length.

A large-signal FET model assumes that the intrinsic device's nonlinearities can be represented by a parallel connection of voltage controlled current sources and charge-based nonlinear capacitors [4-7]. The large-signal equivalent circuit, shown in Fig. 1, uses three charge sources ($Q_{0,g}$, $Q_{0,d}$, $Q_{0,s}$), three current sources ($I_{0,g}$, $I_{0,d}$, $I_{0,s}$), and 8 R-L-C parasitic elements.

The channel current ($I_{0,d}$) is the main nonlinear component in FET models. The presence of thermal and trap effects in FET devices causes great difficulty in modeling $I_{0,d}$. The thermal and trap effects are varied by quiescent bias (V_{gs0}, V_{ds0}) [1-4, 8, 9]. Thus $I_{0,d}$ must be

0-7803-7695-1/03/$17.00 © 2003 IEEE

included the dependence on quiescent bias. If it is assumed that the thermal and trap effects modify the channel current in a multiplicative way, $I_{0,d}$ can be expressed as [1, 4, 9]

$$I_{0,d}(v_{gs}, v_{ds}, V_{gs0}, V_{ds0}) = I_{ds0}(v_{gs}, v_{ds}) \times f_{trap} \times f_{thermal} \quad (1)$$

where I_{ds0} is pulsed I-V at the zero quiescent bias (V_{gs0} = 0 V, V_{ds0} = 0 V). I_{ds0} serves as a reference to describe thermal and trap effects, which means that f_{trap} and $f_{thermal}$ become unity at the bias voltage.

$$f_{trap}\Big|_{V_{gs0}=0,\, V_{ds0}=0} = 1 \quad f_{thermal}\Big|_{V_{gs0}=0,\, V_{ds0}=0} = 1 \quad (2)$$

In case V_{gs0} is lower than the threshold voltage (V_{th}), $f_{thermal}$ becomes unity due to negligible power dissipation.

$$f_{thermal}\Big|_{V_{gs0} < V_{th}} = 1 \quad (3)$$

I_{ds0} is modeled using the curtice equation.

$$I_{ds0}(V_{gs}, V_{ds}) = \beta \cdot V_1^2 \cdot \tanh(\alpha \cdot V_{ds}) \cdot (1 + \lambda \cdot V_{ds}) \quad \text{where} \quad V_1 = V_{gs} - (V_{T0} + \gamma \cdot V_{ds}) \quad (4)$$

Extracted values are given in Table I, and Fig. 2. shows comparison between measured and simulated result.

For the trap and thermal effect characterization (f_{trap}, $f_{thermal}$), pulsed I-V's were measured as the quiescent bias voltages (V_{gs0}, V_{ds0}) were changed.

Fig. 3. shows the pulsed I-V data measured as the gate quiescent bias was changed (V_{gs0} = -1.2, -0.8, -0.6, -0.4 V) with the fixed drain quiescent voltage (V_{ds0} = 0 V). In this condition there are no thermal effect, and the graph shows that the gate quiescent voltage is independent of trap effect. Thus f_{trap} can be expressed as [4, 8]

$$f_{trap} = f(V_{ds0}, v_{gs}, v_{ds}) \quad (6)$$

Fig. 4. shows the pulsed I-V data measured as the drain quiescent voltage was changed (V_{ds0} = 0, 2, 4, 6 V) with the fixed gate quiescent voltage (V_{gs0} = -1.2 V) which was sufficiently low to eliminate the thermal effects.

The differences between each graph are caused by the trap effect. From eq. (1), (2), (3) and (6), f_{trap} can be obtained using

$$f_{trap}(V_{ds0}, v_{gs}, v_{ds}) = \frac{I_{ds}(V_{th}, V_{ds0}, v_{gs}, v_{ds})}{I_{ds}(V_{th}, V_{ds0} = 0, v_{gs}, v_{ds})} \quad (7)$$

where I_{ds} represents the pulsed I-V at the quiescent bias V_{gs0} and V_{ds0}. In our model, the extracted values of f_{trap} were fitted using 5th order b-spline function [6, 10] whose value was determined by V_{ds0}, v_{gs} and v_{ds}.

$f_{thermal}$ is used to account for the channel current variation with the temperature increase due to internal power dissipation (P_{diss}), and it can be expressed as a function of only P_{diss} as follows

$$f_{thermal} = f(P_{diss}) \quad \text{where} \quad P_{diss} = V_{ds0} \cdot I_{ds}^{DC}(V_{gs0}, V_{ds0}) \quad (8)$$

where I_{ds}^{DC} describes DC I-V. The electrical power dissipated in the channel of the device is the principal cause of changes to the electron mobility (μ_n), which in turn reduce the channel current mainly due to degradation in the scatter-limited electron drift velocity. Thus $f_{thermal}$ is related with electron mobility. Since there exists a linear relationship between $log(\mu_n)$ and $log(T)$ [11], and the channel temperature (T) is proportional to the power dissipation (P_{diss}), $f_{thermal}$ can be modeled as

$$log(f_{thermal}) = A + B \times log(P_{diss}) \quad (9)$$

where A and B are fitting parameters.

From eq. (1), (2), (3) and (6), $f_{thermal}$ can be obtained using

$$f_{thermal}(P_{diss}(V_{gs0}, V_{ds0})) = \frac{I_{ds}(V_{gs0}, V_{ds0}, v_{gs}, v_{ds})}{I_{ds}(V_{th}, V_{ds0}, v_{gs}, v_{ds})} \quad (10)$$

Pulsed I-V's for the thermal effect modeling are measured at 20 different quiescent bias voltages covering the range V_{gs0} = –1.2 to –0.4 V, V_{ds0} = 0 to 10 V.

The extracted values of $f_{thermal}$ are used to obtain thermal model parameter A and B in eq. (9), and extracted values are given in Table I.

Current conservation gives the equation of the $I_{0,s}$.

$$I_{0,s} = -(I_{0,g} + I_{0,d}) \quad (11)$$

The parasitic elements (R_g, R_d, R_s, L_g, L_d, L_s, C_{pg}, C_{pd}) are extracted by using a cold FET measurement approach [12-14], and the extracted values are given in Table I. The intrinsic elements are directly calculated from the pulsed I-V's and measured S-parameters at various bias voltages. The partial derivatives of the model element $I_{0,k}$ and $Q_{0,k}$ and delay element τ_{kl} can be described simply in terms of the intrinsic Y-parameters [4, 6, 7].

$$Y_{kl} = \frac{i_k}{v_l} = g_{kl} + \frac{j\omega c_{kl}}{1 + j\omega \tau_{kl}} \approx g_{kl} + \omega^2 c_{kl} \tau_{kl} + j\omega c_{kl} \quad (12)$$

where g_{kl} is the partial derivative of $I_{0,k}$ and c_{kl} is the partial derivative of $Q_{0,k}$. To obtain g_{kl}, c_{kl} and τ_{kl}, S-parameters were measured at 483 different bias voltages covering the range V_{gs0} = -1.2 to -0.1 V, V_{ds0} = 0 to 10 V. The obtained g_{kl}, c_{kl} and τ_{kl} were fitted using 5th order b-spline function whose value was determined by V_{gs0} and V_{ds0}.

III. Simulation vs. Measurement

The model was installed into Agilent ADS using the user-defined model. This was done by compiling the C-code of the extracted model equations.

The model was verified by comparisons with S-parameter at various bias voltages. Fig. 5. shows the comparison between the measured and simulated S-parameter at V_{gs0} = -0.8 V, V_{ds0} = 5 V. The agreement between the modeled and measured data is very good. The obtained RMS error was only 1%. Moreover, the RMS error was kept below 2.5% at every measurement point.

The simulated DC I-V characteristics of the MESFET over the voltage range of V_{gs0} = -1.2 to -0.2 V, V_{ds0} = 0 to 10 V are shown in Fig. 6. During this simulation, V_{gs0} and V_{ds0} followed v_{gs} and v_{ds} respectively in eq. (1). High frequency I-V characteristics of the MESFET at various quiescent bias voltages were also simulated and compared to the measured pulsed I-V's. Fig. 7. shows the simulated

and measured high frequency I-V characteristics at a specific quiescent bias (V_{gs0} = -0.6 V, V_{ds0} = 3 V). Good agreements between the simulated and measured results show that the model is accurate in both DC and high frequency conditions.

The optimum load condition for maximum output power provided by Triquint foundry is 0.913 ∠163.5° at V_{gs0} = -0.63 V, V_{ds0} = 7 V and f = 10 GHz. The output power is 28 dBm and PAE is 51.3 % at the input power of 17.5 dBm. For comparison, single-tone simulation was performed at the same matching condition (Gs = 0.30 ∠151.5°, Gl = 0.913 ∠163.5°). The results are shown in Fig. 8. and matched very well with the measured data.

IV. Conclusion

An improved nonlinear FET model for thermal and trap effects has been introduced and the extraction method of the model parameters has been presented. The model parameters can be extracted using the measured pulsed I-V's and S-parameters at the various quiescent bias voltages. The model shows an excellent agreement between the measured and simulated data in both small-signal and large-signal operations.

Acknowledgement

This work was supported by KOSEF under the ERC program through the MINT research center at Dongguk University.

References

[1] K. Jastrzebski, "Characterisation and modelling of temperature and dispersion effects in power MESFETs," in *24th EuMC*, pp. 1319-1324, 1994.

[2] T. M. Barton, C. M. Snowden, J. R. Richardson, and P. H. Ladbrooke, "Narrow pulse measurement of drain characteristics of GaAs MESFETs," *Electronics Letter*, Vol. 23, pp.68-687, 1987.

[3] Z. Ouarch, J. M. Collantes, J. P. Teyssier, and R. Quere, "Measurement based nonlinear electrothermal modeling of GaAs FET with dynamical trapping effects," Microwave Symposium Digest, *IEEE MTT-S International*, Vol. 2, pp. 599-602, 1998.

[4] K. Koh, H.-M. Park, and S. Hong, "A spline large-signal FET model based on bias-dependent pulsed I-V measurement," *IEEE Trans. Microwave Theory and Techniques*, Vol. 50, No. 11, pp. 2598-2603, 2002.

[5] David E. Root, and Siqi Fan, "Experimental evaluation large-signal modeling assumptions based on vector analysis of bias-dependent S-parameter from MESFETs and HEMTs," *IEEE MIT-S Digest*, Vol. 1, pp. 255-258, 1992.

[6] R. R. Daniels, A. T. Yang, and J. P. Harrang, "A universal large/small signal 3-terminal FET model using a nonquasi-static charge-based approach," *IEEE Trans. Electron Devices*, Vol. 40, No. 10, pp. 1723-1729, 1993.

[7] Daniel Roques, Francis Brasseau, Bernard Cogo, Michel Soulard, and Jean-Louis Cazaux, "A non quasi-static non-linear p-HEMT model operating up to millimetric frequencies," *ELECTRONICS LETTERS*, Vol. 36, No. 10, pp. 857-858, May 2000.

[8] T. M. Barton, C. M. Snowden, J. R. Richardson, and P. H. Ladbrooke, "Narrow pulse measurement of drain characteristics of GaAs MESFETs," *Electronics Letter*, Vol. 23, pp.68-687, 1987.

[9] P. H. Ladbrooke, A. K. Jastrzebski, R.J. Donarski, J.P. Bridge, and J. E. Barnaby, "Mechanism of drain current droop in GaAs MESFETs," *Electronics Letter*, Vol. 31, No. 21, pp. 1875-1876, 12 Oct. 1995.

[10] C. de Boor, *A Practical Guide to Splines*, New York: Springer-Verlag, 1978.

[11] O. Madelung, *Data in Science and Technology: Semiconductors - Group IV Elements and III-V Compounds*, New York: Springer-Verlag, pp. 106, 1991.

[12] Gilles Dambrine, Alain Cappy, Frederic Heliodore, and Edouard Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory and Techniques*, Vol. 36, No. 7, pp. 1151-1159, July 1988.

[13] Manfred Berroth and Roland Bosch, "High-frequency equivalent circuit of GaAs FET's for large-signal applications," *IEEE Trans. Microwave Theory and Techniques*, Vol. 39, No. 2, pp. 224-229, Feb. 1991.

[14] Paul M. White, and Richard M. Healy, "Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from Coldfet Measurements," *IEEE Microwave and Guided Wave Letters*, Vol. 3, No. 12, pp. 453-454, Dec. 1993.

TABLE I
EXTRACTED MODEL PARAMETERS

Parameter	Value	Parameter	Value
V_{T0}	-1.06 V	R_g	0.82 Ω
γ	-0.012	R_d	0.89 Ω
β	240 mA/V	R_s	0.72 Ω
α	2.1	L_g	25.0 pH
λ	0.0028 V^{-1}	L_d	52.0 pH
Q	1.87	L_s	9.2 pH
A	0.0156	C_{pg}	69 fF
B	-1.0162	C_{pd}	170 fF

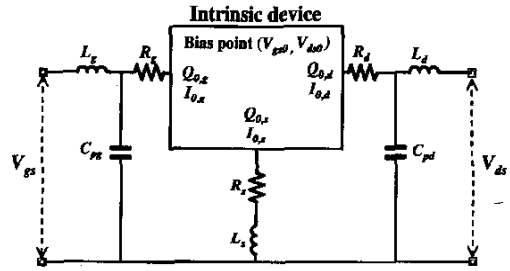

Fig. 1. Schematic of the FET large signal model

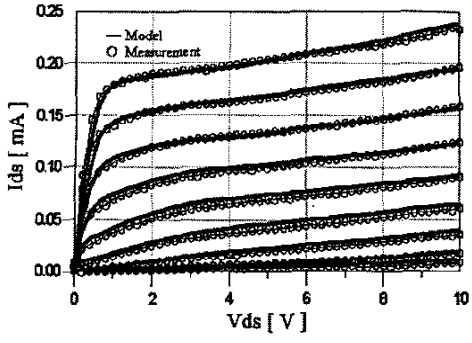

Fig. 2. Measured and simulated I_{ds0}

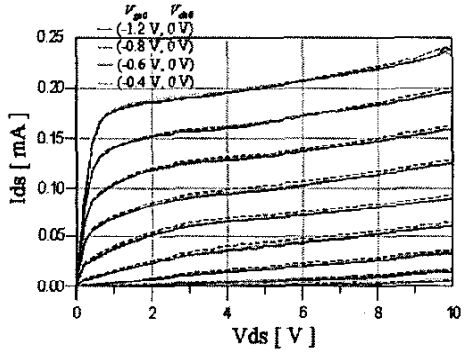

Fig. 3. Pulsed I-V's measured as the gate quiescent bias was swept while the drain quiescent bias was fixed

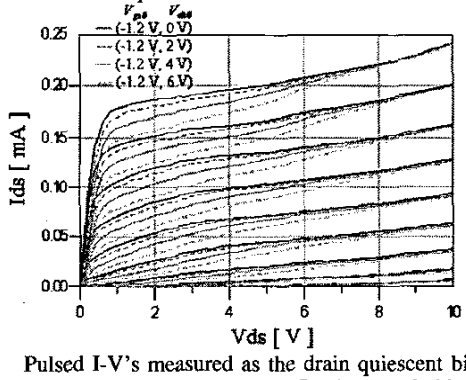

Fig. 4. Pulsed I-V's measured as the drain quiescent bias was swept while the gate quiescent bias was fixed at threshold voltage

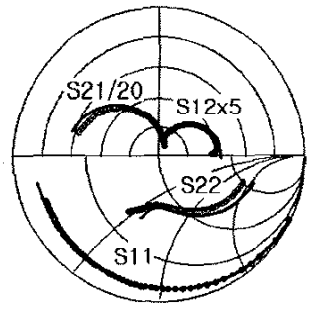

Fig. 5. Measured (circle) and simulated (line) S-parameter at V_{gs0} = -0.8 V and V_{ds0} = 5 V (f = 0.5 ~ 15 GHz)

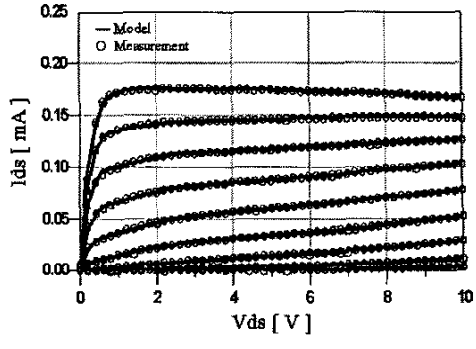

Fig. 6. Measured and simulated DC I-V

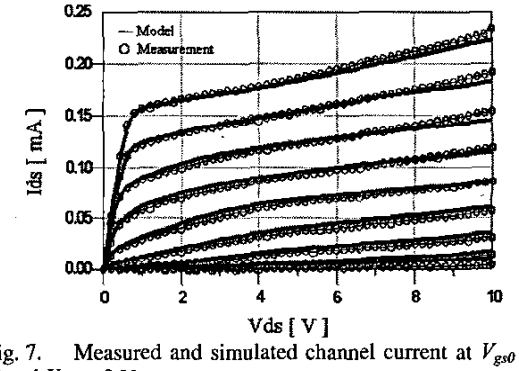

Fig. 7. Measured and simulated channel current at V_{gs0} = -0.6 V and V_{ds0} = 3 V

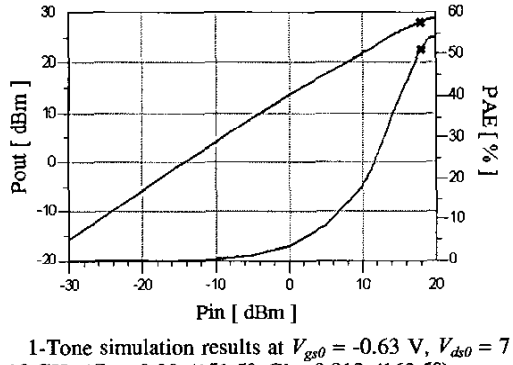

Fig. 8. 1-Tone simulation results at V_{gs0} = -0.63 V, V_{ds0} = 7 V and f = 10 GHz (Gs = 0.30∠151.5°, Gl = 0.913∠163.5°)